CLAIMS

What is claimed is:

1. A method for optimizing a plurality of numerically controlled delay lines (NCDLs) in a DDR memory controller, the method comprising:

(a) acquiring a plurality of statistics, the plurality of statistics defining an operating region for the DDR memory controller; and

(b) calculating optimal values for the plurality of NCDLs, the optimal values calculated using the plurality of statistics.

2. The method of claim 1, wherein the plurality of NCDLs comprise at least one of a write NCDL, a read NCDL, and a gate NCDL.

3. The method of claim 2, wherein the plurality of statistics comprise a write NCDL offset, the write NCDL offset complimenting a delay locked loop output value and enabling the write NCDL to phase shift a data strobe write signal with respect to an outgoing data signal.

4. The method of claim 2, wherein the plurality of statistics comprise a read NCDL offset, the read NCDL offset complimenting a delay locked loop output value and enabling the read NCDL to phase shift a data strobe read signal with respect to an incoming data signal.

5. The method of claim 2, wherein the gate NCDL enables phase shifting a data strobe read signal with respect to the DDR memory controller's internal clock signal.

6. The method of claim 2, wherein the plurality of statistics comprise a passing count value, the passing count value associated with a number of working combinations of read NCDL values and write NCDL values for a given gate NCDL value.

7. The method of claim 1, wherein the plurality of statistics is acquired by running a simultaneously switched outputs test on the DDR memory controller.

8. The method of claim 7, wherein the simultaneously switched outputs test is performed at least once for each combination of NCDL values for the plurality of NCDLs.

9. The method of claim 1, wherein the optimal values comprise a final gate NCDL value.

10. The method of claim 9, wherein the final gate NCDL value is a function of a corner gate value, the corner gate value associated with a passing count value.

11. The method of claim 9, wherein the final gate NCDL value is a function of a delay locked loop output value.

12. The method of claim 1, wherein the optimal values comprise a final read NCDL value.

13. The method of claim 12, wherein the final read NCDL value is a function of a final gate NCDL value.

14. The method of claim 12, wherein the final read NCDL value is a function of a plurality of read NCDL values.

15. The method of claim 1, wherein the optimal values comprise a final write NCDL value.

16. The method of claim 15, wherein the final write NCDL value is a function of a plurality of write NCDL values.

17. A computer readable media storing a plurality of instructions, wherein execution of the plurality of instructions causes:

(a) acquiring a plurality of statistics, the plurality of statistics defining an operating region for a DDR memory controller; and

(b) calculating optimal values for a plurality of numerically controlled delay lines (NCDLs) in the DDR memory controller, the optimal values calculated using the plurality of statistics.

18. The computer readable media of claim 17, wherein the plurality of NCDLs comprise at least one of a write NCDL, a read NCDL, and a gate NCDL.

19. The computer readable media of claim 18, wherein the plurality of statistics comprise a write NCDL offset, the write NCDL offset complimenting a delay locked loop output value and enabling the write NCDL to phase shift a data strobe write signal with respect to an outgoing data signal.

20. The computer readable media of claim 18, wherein the plurality of statistics comprise a read NCDL offset, the read NCDL offset complimenting a delay locked loop output value and enabling the read NCDL to phase shift a data strobe read signal with respect to an incoming data signal.

21. The computer readable media of claim 18, wherein the gate NCDL enables phase shifting of the internal clock generated gate signal with respect to the DDR device DQS signal, so as to enable the incoming DQS for read data capture.

22. The computer readable media of claim 18, wherein the plurality of statistics comprise a passing count value, the passing count value associated

with a number of working combinations of read NCDL values and write NCDL values for a given gate NCDL value.

23. The computer readable media of claim 17, wherein the plurality of statistics is acquired by running a simultaneously switched outputs test on the DDR memory controller.

24. The computer readable media of claim 23, wherein the simultaneously switched outputs test is performed at least once for each combination of NCDL values for the plurality of NCDLs.

25. The computer readable media of claim 17, wherein the optimal values comprise a final gate NCDL value.

26. The computer readable media of claim 25, wherein the final gate NCDL value is a function of a corner gate value, the corner gate value associated with a passing count value.

27. The computer readable media of claim 25, wherein the final gate NCDL value is a function of a delay locked loop output value.

28. The computer readable media of claim 17, wherein the optimal values comprise a final read NCDL value.

29. The computer readable media of claim 28, wherein the final read NCDL value is a function of a final gate NCDL value.

30. The computer readable media of claim 28, wherein the final read NCDL value is a function of a plurality of read NCDL values.

31. The computer readable media of claim 17, wherein the optimal values comprise a final write NCDL value.

32. The computer readable media of claim 31, wherein the final write NCDL value is a function of a plurality of write NCDL values.